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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,359	09/19/2003	Chi-Chun Chen	2001-1488 / 24061.431	8170
43717 7590 11/19/2008 HAYNES AND BOONE, LLP IP Section 2323 Victory Avenue Suite 700 Dallas, TX 75219				
EXAMINER				
SMITH, FRANCIS P				
ART UNIT		PAPER NUMBER		
1792				
MAIL DATE		DELIVERY MODE		
11/19/2008		PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/666,359

**Applicant(s)**

CHEN ET AL.

**Examiner**

Francis P. Smith

**Art Unit**

1792

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 19 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-41 and 43 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-41 and 43 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)
- Paper No(s)/Mail Date \_\_\_\_\_

- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 18, 2008 has been entered.

### ***Response to Arguments***

2. Applicants argue that Raaijmakers process is distinct from a plasma process such that the presence of radicals does not necessitate plasma. However, Raaijmakers distinctly and clearly states that radicals (e.g. utilized in the nitridation and re-oxidation steps) are created by a plasma generator (e.g. a plasma nitridation/reoxidation process) (col. 8, lines 36-40; col. 20, lines 41-46, line 64-col. 21, line4).

As per claim 25, applicants argue that the claim "clearly requires the plasma reoxidation process occur in the presence of a material selected from the group consisting of O<sub>2</sub>, N<sub>2</sub>O, and NO". Claim 25 of the instant application, however, pertains to oxide and nitride layer thicknesses, and thus, applicants' arguments are apparently without merit.

Claims 1, 2, 12, 14, 16, 18, 23, 34, 38, and 40 are listed as being amended;

however, claims 1, 2, 12, 23, and 34 appear amended in the current listing of claims. Claim 42 is canceled. Claims 1-41 and 43 are currently pending and examined on the merits.

***Claim Rejections - 35 USC § 103***

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
4. Claims 1, 2-24, 26-41, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raaijmakers et al. (US 6,348,420).

For claims 1 and 23, Raaijmakers teaches processes for forming ultra thin dielectric stacks of high quality. First, a wafer is cleaned to provide a clean silicon surface (i.e. providing a silicon substrate) col. 13, lines 43-45. Then, the method includes loading the said substrate into a processing chamber at 780°C where a first oxide layer grows on the semiconductor structure (i.e. thermal oxide layer) col. 13, lines 57-59. A silicon nitride layer is then deposited over the thermal oxide layer forming a stacked gate dielectric (col. 3, lines 20-35). During an anneal step, the substrate is exposed to a nitriding agent (i.e. nitridation process) followed by exposure to an oxidizing agent (e.g. reoxidation comprising  $N_2O$ , NO,  $O_2$ , or O radicals) (col. 15, lines 21-37). A remote plasma generator is located upstream from the reaction chamber and is connected to each gas line via separate mass flow controller and valves, allowing for said plasma nitridation/reoxidation processes (col. 7, lines 44-65).

Raaijmakers does not expressly state a plasma reoxidation process at a

temperature at or below approximately 700°C. However, Raaijmakers teaches depositing a dielectric layer at a temperature of 650-700°C. **Raaijmakers further states that all of the remaining processes are conducted under similar or identical temperature and pressure (col. 19, lines 18-34).** Therefore, as suggested by Raaijmakers, it would have been well within the level of ordinary skill in the art to subject the intermediate stacked gate dielectric to a reoxidation process at a temperature at or below approximately 700°C. Regarding the plasma nitridation and re-oxidation steps, Raaijmakers clearly teaches the use of a plasma generator to create radicals (e.g. for said nitridation and re-oxidation steps). Specifically, Raaijmakers teaches the use of a plasma generator for the purpose of providing excited species (col. 8, lines 36-40). Subsequent deposition, a densification process is performed utilizing N<sub>2</sub>O and N radicals (e.g. obtained by passing process gas through a plasma generator) at an anneal/densification temperature of 680°C (i.e. plasma nitridation/reoxidation) (col. 17, lines 48-56; col. 20, line 64-col. 21, line 4).

Regarding claims 2 and 24, Raaijmakers teaches a processes where the thermal oxide layer grows to about 0.5 nm (or 5 angstroms) while the silicon nitride layer grows to about 3 nm (or 30 angstroms) (col. 14, lines 3-5, 19-21).

For claims 4-7 and 26-29, Raaijmakers teaches a processes for forming ultra thin dielectric stacks of high quality where the dielectric growth and deposition steps (i.e. formation of the thermal silicon oxide and nitride layers) are conducted in the rage of 650-850°C (col. 11, lines 7-23).

As per claims 8 -10 and 30-32, Raaijmakers teaches a process for forming ultra

thin dielectric stacks of high quality where oxide layer is a thermal silicon oxynitride and the CVD nitride layer consists of silicon nitride (col. 11, lines 25-29; col. 14, lines 1-5, 18-21).

Regarding claims 11 and 33, Raaijmakers teaches a method of forming a nitride layer by a remote plasma enhanced (RPECVD) process. (col. 18, lines 34-46).

For claims 12-15 and 34-37, Raaijmakers discloses a process for forming ultra thin dielectric stacks of high quality where the plasma nitridation process is conducted at a temperature range of 650-680°C in a reaction chamber set within a range of 1-80 torr (col. 20, lines 34-36; col. 19, lines 22-26). Furthermore, Raaijmakers discloses providing N<sub>2</sub> during a nitridation anneal step (col. 15, lines 35-37; col. 20, lines 44-46).

As for claims 20, 21 and 43, Raaijmakers teaches a process for forming ultra thin dielectric stacks of high quality aided by plasma energy with an optional anneal step using nitriding or oxidizing agents (i.e. reoxidation step). The oxidant may be N<sub>2</sub>O, NO, or O<sub>2</sub> (col. 11, lines 38-52; col. 17, lines 66-67; col. 20, lines 64-67).

Regarding claims 16-19 and 38-41, Raaijmakers teaches a process for forming ultra thin dielectric stacks of high quality aided by plasma energy with an optional anneal step using nitriding or oxidizing agents (i.e. reoxidation step). The oxidant may be comprised of N<sub>2</sub>O, NO, or O<sub>2</sub> (col. 11, lines 38-52; col. 17, lines 66-67; col. 20, lines 64-67). For deposition processes, the wafer is preferably kept at a temperature below about 750°C in a chamber with a pressure range of 1-80 torr (col. 19, lines 22-26; col. 20, lines 19-21).

Although Raaijmakers states that the processing steps conducted in situ are

conducted under similar or identical temperatures and pressures (col. 19, lines 18-22,) Raaijmakers is silent with regard to a specific temperature and pressure range during the reoxidation step. However, It would be obvious to one skilled in the art at the time of the invention to maintain the parameters of the reactor chamber at the temperature and pressure of the silicon oxynitride and nitride deposition during the annealing (reoxidation) step in order to avoid pressure/temperature ramping and minimize thermal stress that could cause peeling of coatings from the substrate.

5. Claims 3 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raaijmakers et al. (US 6,348,420) in view of Bloom et al. (US 6,228,779).

For claims 3 and 25, Raaijmakers teaches processes for forming ultra thin dielectric stacks of high quality. A thermal oxide layer grows to about 0.5 nm (or 5 angstroms) while the silicon nitride layer is about 3 nm (or 30 angstroms) col. 14, lines 3-5, 19-21. Raaijmakers, however is silent regarding a nitride layer of 5-15 angstroms.

Bloom teaches a method of forming a dense and stable dielectric layer of silicon nitride and silicon dioxide for use in transistors of ULSI circuits where the nitride layer is placed above the silicon dioxide layer. The said silicon nitride layer may be in a range of 5-20 angstroms (col. 3, lines 15-16). It would be obvious to one skilled in the art at the time of the invention to modify Raaijmakers' method by incorporating Bloom's nitride layer thickness in order to find the optimum nitride layer thickness for preventing the migration of dopants such boron into the silicon dioxide dielectric layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Francis P. Smith whose telephone number is (571) 270-3717. The examiner can normally be reached on Monday through Thursday 7:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mikhail Kornakov can be reached on (571) 272-1303. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/F. P. S./  
Examiner, Art Unit 1792  
/Michael Kornakov/  
Supervisory Patent Examiner, Art Unit 1792